# REVIEW OF THE HURDLES YOU NEED TO JUMP TO USE AN FPGA IN HEP

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# IN THE BEGINNING…

- … the FPGA was empty and without form

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IPbus and uHAL provide transport layers for

- Ethernet
- PCIe
- AXI chip-to-chip

communication to the FPGA

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IPbus allows simple, high-performance communication to our firmware components without needing to worry about how we drive the bus

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The EMP framework separates out the clocking and triggering infrastructure

LHC-like timing available out-of-the-box

Neatly-contained for other experiments

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The EMP framework provides infrastructure for injecting and capturing data in the chip

And also for running that same data through the same algorithm in the simulator

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The EMP framework allows injection and capture of data on the links

And supports the transparent insertion and stripping of a number of different error-checking protocols

**EVEN IF I DIDN'T GET IT WORKING ON THE KCU105 IN TIME**

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All modules in the firmware include IPbus readable revision numbering

IPBB allows no-human-required building of bitfiles
The IPBB package contains a list of MD5 hashes on the source files, along with the bit file, to verify that the correct file versions were used

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IPBB is a fully open-source build tool with an understanding of how to use sources distributed across multiple GIT and/or SVN repositories

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SMASH - not really part of EMP
but a neat tool for rapidly and reliably
controlling diverse hardware

Ran out of time to cover it!

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By changing one line in your dep file you can port your design to a different hardware platform

# THE END
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